9. (Amended) The apparatus of claim 6, wherein the processor is further adapted to: interact with the interface to receive the key from the computer system.

16. (Amended) The microprocessor of claim 15, wherein the execution unit comprises:

a control unit; and

a memory coupled to the control unit and storing microcode to cause the control unit to use the key and the identifier to produce the hash value.

Add the following new claims:

21. (New) The method of claim 2, wherein the processor number identifies a microprocessor of the second computer system.

22. (New) The method of claim 21, wherein the processor number uniquely identifies the microprocessor.

23. (New) The computer system of claim 7, wherein the processor number identifies a microprocessor of the first computer system.

24. (New) The computer system of claim 23, wherein the processor number uniquely identifies the microprocessor.

25. (New) The article of claim 14, wherein the processor number identifies a microprocessor of the first system.

26. (New) The article of claim 25, wherein the processor number uniquely identifies the microprocessor.